

What is Claimed is:

1 1. During the testing of the operation of processing
2 unit, a system for identifying the occurrence of a
3 processor unit program code flush condition in the pipeline
4 flattener, the system comprising:

5 timing trace apparatus responsive to signals from the
6 processor unit, the timing trace apparatus generating a
7 timing trace stream;

8 program counter trace apparatus responsive to signals
9 from the processing unit, the program counter trace
10 apparatus generating a program counter trace stream; and

11 synchronization apparatus applying periodic signals to
12 the timing trace apparatus and to the program counter trace
13 apparatus, the periodic signals resulting in periodic sync
14 markers in the timing trace stream and in the program
15 counter trace stream.

16 wherein the program counter trace apparatus is
17 responsive to a program code flush signal, the program
18 counter trace apparatus generating sync marker signal group
19 identifying the occurrence of the program code flush signal
20 and relating the program code flush signal to the timing
21 trace stream and to the program code execution.

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23 2. The system as recited in claim 1 wherein the
24 marker signal group includes a program counter address, a
25 timing index and a periodic sync ID.

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2 3. The system as recited in claim 1 further
3 comprising:

4 data trace apparatus responsive to signals from the
5 processing unit, the data trace apparatus generating a data
6 trace stream, wherein the periodic signals are applied to
7 the data trace apparatus resulting in periodic sync markers
8 in the data trace stream; and

9 a host processing unit, the host processing unit
10 responsive to the timing trace stream, the program counter
11 trace stream and the data trace stream, the host processing
12 unit reconstruction the processing activity of the
13 processing unit from the trace streams.

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15 4. The method for communicating an occurrence of a
16 program code flush signal from a target processor unit to a
17 host processing unit, the method comprising:

18 generating a timing trace stream, a program counter
19 trace stream, and data trace stream, and

20 in the program counter trace stream, including a
21 program code flush sync marker signal group indicating an
22 occurrence of program code flush signal and relating the
23 occurrence to the data trace stream and to the timing trace
24 stream.

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26 5. The method as recited in claim 4 further
27 including:

1 including periodic sync markers in the timing trace
2 stream and in the program counter trace stream; and
3 including in the program code sync marker reference to
4 a periodic sync marker.

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6 6. In a processing unit test environment wherein a
7 target processor transmits a plurality of trace streams to
8 a host processing unit, a program code flush sync marker
9 signal group included in a trace signal stream, the marker
10 signal group comprising:

11 indicia of the occurrence of a program code flush
12 signal;

13 indicia of the relationship of the occurrence of the
14 program code flush signal to the target processor clock;
15 and

16 indicia of the relationship of the occurrence of the
17 program code flush signal to the target processor program
18 execution.

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20 7. In a target processing unit generating trace test
21 signals for transfer to a host processing unit, a program
22 counter trace generation apparatus comprising:

23 sync marker assembly apparatus, the sync marker
24 assembly apparatus including:

25 a storage unit;

26 a decoder unit responsive to a program code flush
27 signal for storing an indicia of the program code flush

1 signal in the storage unit, the decoder unit generating a
2 controls signal;

3 a gate unit having a timing index, a periodic
4 sync signal, and a program counter address, the gate unit
5 storing the timing index, the periodic sync signal and the
6 program counter address in the storage unit; and

7 a FIFO unit, the storage unit transferring the
8 stored signals to the FIFO unit in the form of a program
9 code flush sync marker.

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11 8. The program counter trace apparatus as recited in
12 claim 7 responsive to a selected control signal for
13 transferring program code flush marker in the FIFO unit to
14 an output port of the target processor.

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16 9. The program counter trace apparatus as recited in
17 claim 8 wherein the apparatus can form a periodic sync
18 marker in response to a periodic sync signal.

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20 10. The program counter trace apparatus as recited in
21 claim 9 wherein the program code flush signal indicates the
22 change from a first instruction code sequence to a second
23 instruction code sequence in the pipeline flattener.

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25 11. The program counter trace apparatus as recited in
26 claim 10 wherein the first instruction code sequence is a

1 program instruction code and the second instruction
2 sequence is an interrupt service routine.

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